Amendments to the Claims:

The following Listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently amended) A semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer, comprising in order:

providing a fluid surface protecting layer ~~which can be hardened by light or heat~~,

coating the fluid surface protecting layer on the circuit side of the semiconductor wafer,

placing a polymeric film material over the fluid surface protecting layer,

hardening said fluid surface protecting layer by exposure to radiation or upon heating, and

grinding said semiconductor wafer,

wherein grinding said semiconductor wafer is done after hardening said fluid surface protecting layer.

2. (Previously presented) A semiconductor surface protecting method according to claim 1, whereby the coating, placing, and hardening steps are carried out in a vacuum.

3. (Cancelled)

4. (Previously presented) A semiconductor surface protecting method according to claim 1, wherein, before hardening the fluid surface protective layer, the fluid surface protective layer has an elastic shear loss modulus (G") less than its elastic shear storage modulus (G') at room temperature (20-25°C) and an elastic shear loss modulus (G") greater than its elastic shear storage modulus (G') at 30-100°C, as measured with a viscoelasticity measuring apparatus at a frequency of 10 Hz, a deformation of 0.04% and a temperature ramp rate of 3°C/min., and the surface protective layer after hardening has an elastic tensile storage modulus (E') at 50°C greater

than 5×10^7 Pa as measured with a viscoelasticity measuring apparatus at a frequency of 1 Hz, a deformation of 0.04% and a temperature-ramp rate of 5°C/min.

5. (Previously presented) A semiconductor surface protecting method according to claim 1, wherein the fluid surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compounds being selected from the group consisting of:

(1) (meth)acrylic-based low molecular weight compounds, selected from isocyanuric acid-derived (meth)acrylates, pentaerythritol-derived (meth)acrylates or bisphenol A-derived (meth)acrylates, which are crystalline or waxy at room temperature (20-25°C),

(2) urethane (meth)acrylate resins of molecular weight 10,000 or greater which are solid at room temperature (20-25°C), and

(3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins, cresol-novolac epoxy (meth)acrylate resins and bisphenol A epoxy di(meth)acrylate resins.

6. (Previously presented) A semiconductor surface protecting method according to claim 5, wherein the fluid surface protecting layer further contains a free-radical polymerization initiator.

7. (Previously presented) A semiconductor surface protecting surface method according to claim 1, wherein the fluid surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the molecule, the cationically polymerizable compounds being selected from the group consisting of:

(1) epoxy-based low molecular compounds, selected from hydroquinone diglycidyl ether or diglycidyl terephthalate, which are crystalline or waxy at room temperature (20-25°C), and

(2) phenol-novolac epoxy resins, cresol-novolac epoxy resins and bisphenol A epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

8. (Previously presented) A semiconductor surface protecting method according to claim 7, wherein the fluid surface protecting layer further contains a cationic polymerization initiator.

9. (Previously presented) A semiconductor surface protecting method according to claim 4, wherein the surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compounds being selected from the group consisting of:

(1) (meth)acrylic-based low molecular weight compounds, selected from isocyanuric acid-derived (meth)acrylates, pentaerythritol-derived (meth)acrylates or bisphenol A-derived (meth)acrylates, which are crystalline or waxy at room temperature (20-25°C),

(2) urethane (meth)acrylate resins of molecular weight 10,000 or greater which are solid at room temperature (20-25°C), and

(3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins, cresol-novolac epoxy (meth)acrylate resins and bisphenol A epoxy di(meth)acrylate resins.

10. (Previously Presented) A surface protecting sheet according to claim 9, wherein the fluid surface protecting layer further contains a free-radical polymerization initiator.

11. (Previously presented) A semiconductor surface protecting method according to claim 4, wherein the fluid surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the molecule, the cationically polymerizable compounds being selected from the group consisting of:

(1) epoxy-based low molecular compounds, selected from hydroquinone diglycidyl ether or diglycidyl terephthalate, which are crystalline or waxy at room temperature (20-25°C), and

(2) phenol-novolac epoxy resins, cresol-novolac epoxy resins and bisphenol A epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

12. (Previously presented) A semiconductor surface protecting method according to claim 11, wherein the surface protecting layer further contains a cationic polymerization initiator.

13. (New) A semiconductor surface protecting method according to claim 1, whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer, comprising in order:

providing a fluid surface protecting layer,

coating the fluid surface protecting layer on the circuit side of the semiconductor wafer,

placing a polymeric film material over the fluid surface protecting layer,

hardening said fluid surface protecting layer by exposure to radiation, and

grinding said semiconductor wafer,

wherein grinding said semiconductor wafer is done after hardening said fluid surface protecting layer.